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IN THE CLAIMS:

1. (Currently Amended) An image processing apparatus comprising:

at least two signal processor modules interconnected with each other in series, each of the signal processor modules having an input port through which data is input, a memory which stores data, a signal processor portion which carries out processing on input data according to a program and an output port through which data is output,

wherein at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data,

wherein said at least one of the signal processor modules stores within predetermined temporal periods in the memory unprocessed input data as input through the input port and processed data obtained by reading out and processing unprocessed input data stored in the memory a predetermined number of cycles before and outputs within the predetermined temporal periods through the output port unprocessed data and processed data stored in the memory the predetermined number of cycles before, and

wherein the other signal processor module(s) stores within predetermined temporal periods in the memory unprocessed input data as input through the input port and processed data obtained by reading out and processing unprocessed input data stored in the memory a predetermined number of cycles before and outputs within the predetermined temporal periods through the output port processed data stored in the memory the predetermined number of cycles before, or stores in the memory unprocessed input data as input through the input port and outputs through the output port unprocessed input data stored in the memory the predetermined number of cycles before.

2. (Canceled)

3. (Currently Amended) The image processing apparatus according to Claim [[2]] 1, further comprising:

a synchronous circuit which causes data transfer between signal processor modules to occur in synchronization with clocks which are the same in phase and frequency.

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4. (Previously Presented) The image processing apparatus according to Claim 3, wherein the data transfer widths between the signal processor modules are equal to each other and the synchronous circuit determines the frequency of the transfer clock on the basis of the data transfer rate between the pair of signal processor modules between which the largest amount of data is to be transferred.

5. (Currently Amended) ~~The image processing apparatus according to Claim 1,~~
~~further comprising~~ An image processing apparatus comprising:
at least two signal processor modules interconnected with each other in series, each of
the signal processor modules having an input port through which data is input, a memory
which stores data, a signal processor portion which carries out processing on input data
according to a program and an output port through which data is output;
a mounting means, on which a signal processor module is removably mounted,
provided for at least one of the signal processor modules; and
a switching means ~~[[is]]~~ provided for said at least one signal processor module to
transfer data to the signal processor module through its input port when it is mounted on the
mounting means and to transfer the same to a component forward of the signal
processor module when it is not mounted on the mounting means,
wherein at least one of the signal processor modules outputs in parallel both
unprocessed input data and processed data obtained by processing the input data.